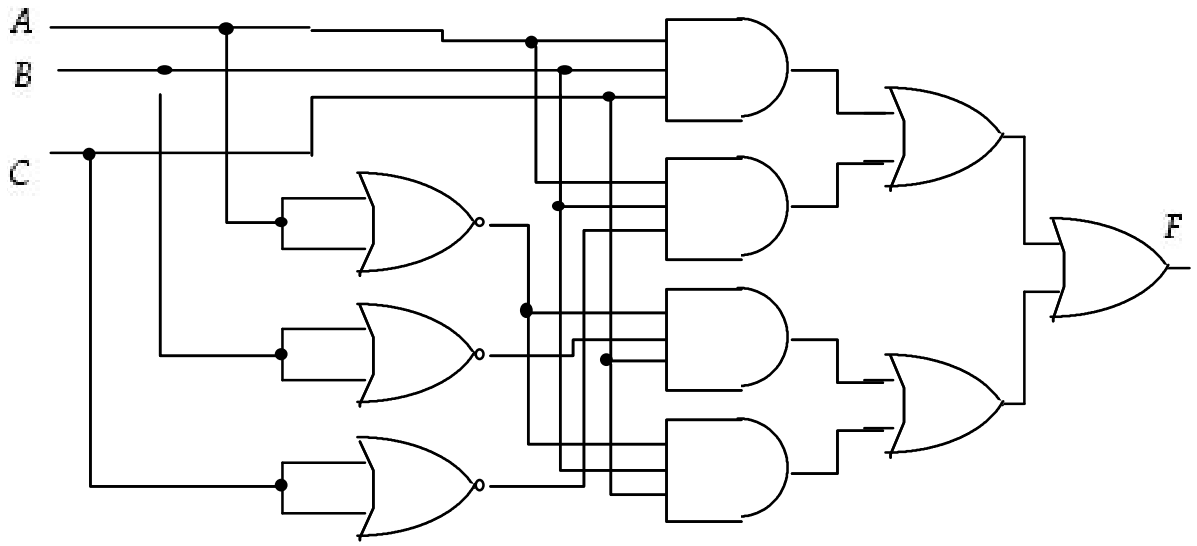
Answer THREE questions

The numbers in square brackets in the right-hand margin indicate the provisional allocation of maximum marks per sub-section of a question.

1. State *De Morgan's theorems* and demonstrate their validity using a truth table. [2]

   Write out the truth tables for each of the following 2-input logic gates:
   AND, OR, NAND, NOR, XOR. [2]

   Write down an expression for the output *F* of the circuit below and draw up a truth table that specifies its performance. [4]

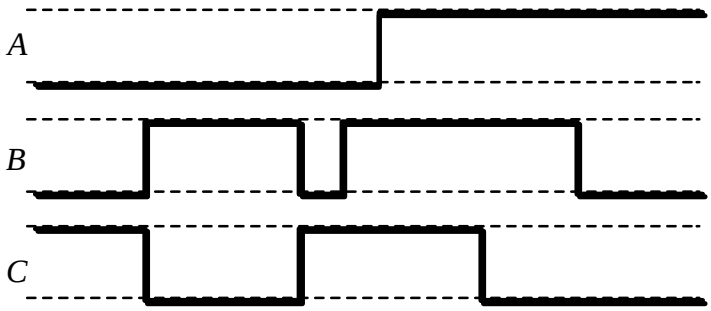


Simplify the logic using a Karnaugh Map and show how the circuit can be implemented using

(i) two 2-input AND gates, an OR gate and a NOR gate;

(ii) NAND logic only, with as few gates as possible. [8]

The inputs *ABC* change as shown:



Sketch the output *F* and show at which point the circuit may be subject to a *static hazard*. What additional logic could be used to eliminate this possibility? [4]

PLEASE TURN OVER

2. Sketch the circuit for a scale-of-8 *asynchronous counter*, implemented using JK flip flops connected as T flip flops, which can be set by an input *P* to count up or down. Explain its mode of operation in terms of the mode of operation of an individual JK flip flop connected as a T flip flop. [8]

A *synchronous counter* is required to count up to 5 and then reset to 1. Draw the required *truth table* and hence devise the *change function* for each of the three flip flops. Sketch a circuit which implements this function using JK flip flops. You may assume that the change function of a JK flip flop is $CF = J\overline{Q} + KQ$. [12]

3. Outline the behaviour of the *analogue comparator* and explain its importance for analogue-to-digital conversion circuits. [4]

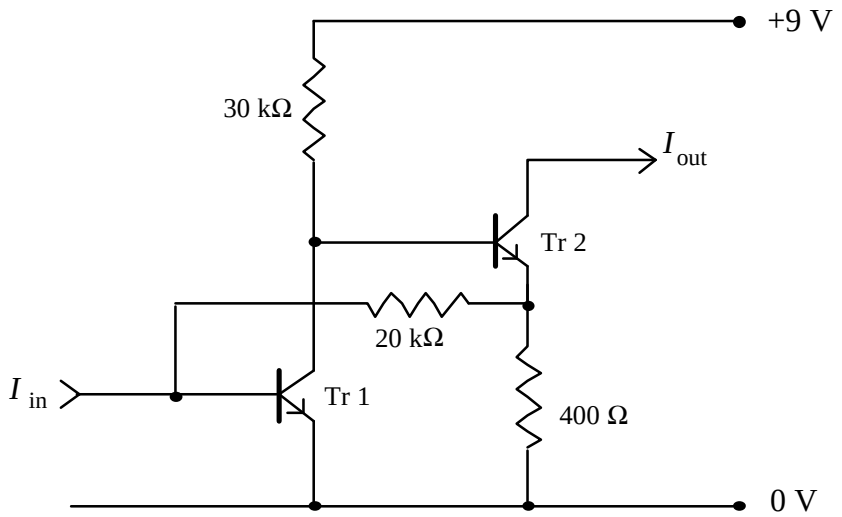
Describe the principles of operation and relative advantages of
(i) the successive approximation ADC,
(ii) the flash ADC,
(iii) the integrating ADC. [16]

4. The circuit shown below forms a current amplifier with negative feedback. Find the D.C. quiescent current in the two transistors when I_{in} is zero. For each transistor assume $\beta \bullet 100$ and $V_{BE} \bullet 0.6$V, and make any other reasonable approximations, which you should justify. [6]

Using these same approximations, find the two extreme values of the output current and the corresponding values for the input current. [6]

Hence estimate the large-signal current gain. [2]

Calculate the output voltage when a load of 1 kΩ is connected from the output to the 9V line and 1 MΩ is connected between the input and the 0V line. [6]



CONTINUED

5. Describe the concept of voltage-derived negative feedback as applied to amplifier circuits, giving examples of both series-applied and parallel-applied feedback. Include explanations of the terms *series-applied feedback*, *parallel-applied feedback*, and *virtual earth*. [8]

Explain how the addition of negative feedback to a basic amplifier affects its gain, input impedance, output impedance and frequency response. [12]

END OF PAPER