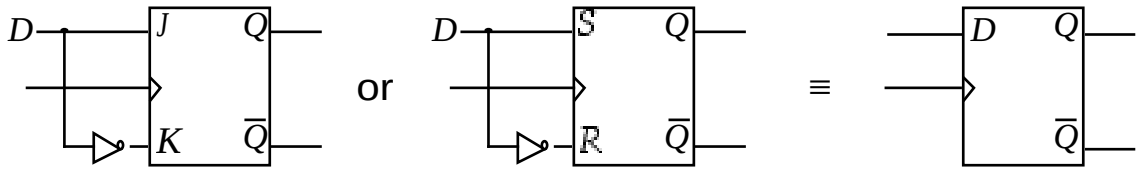
Week 6: More Sequential Logic, Memory, Analogue Converters

6.1 Shift Registers

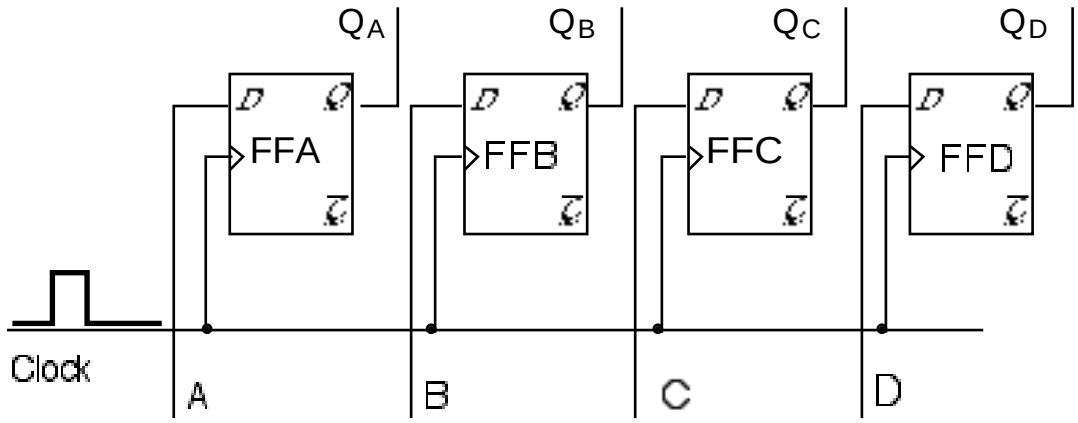
Shift registers are memory devices which consist of a series of flip flops, generally of the JK or SR type connected as D flip flops.



Recall that (for a positive edge clocked flip flop) a clock pulse transfers the input *D* logic level to the output *Q*.

6.1.1 Parallel-In Parallel-Out (PIPO)

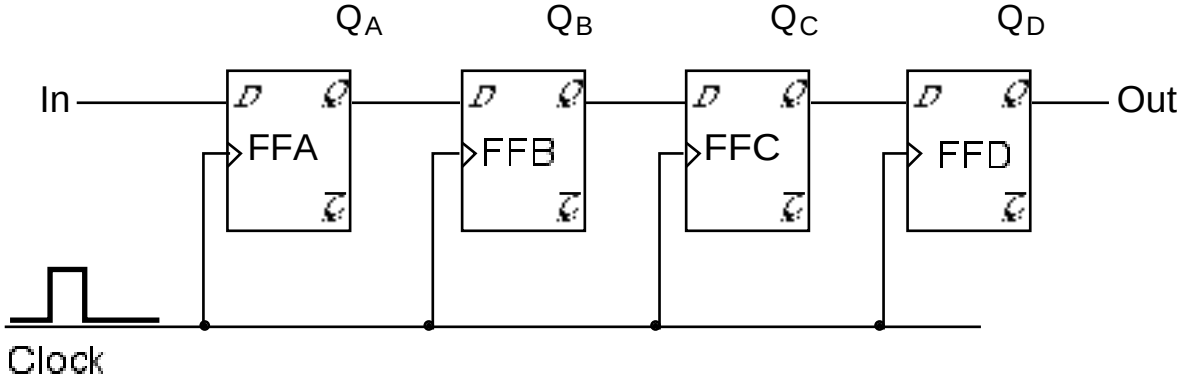
The circuit below "reads in" 4 bits when the clock pulse occurs (actually on its rising edge). After the clock pulse has occurred the pattern of values that were at the input is held – i.e. stored – at the outputs until another pulse occurs.



The input pattern is *shifted* to the outputs.

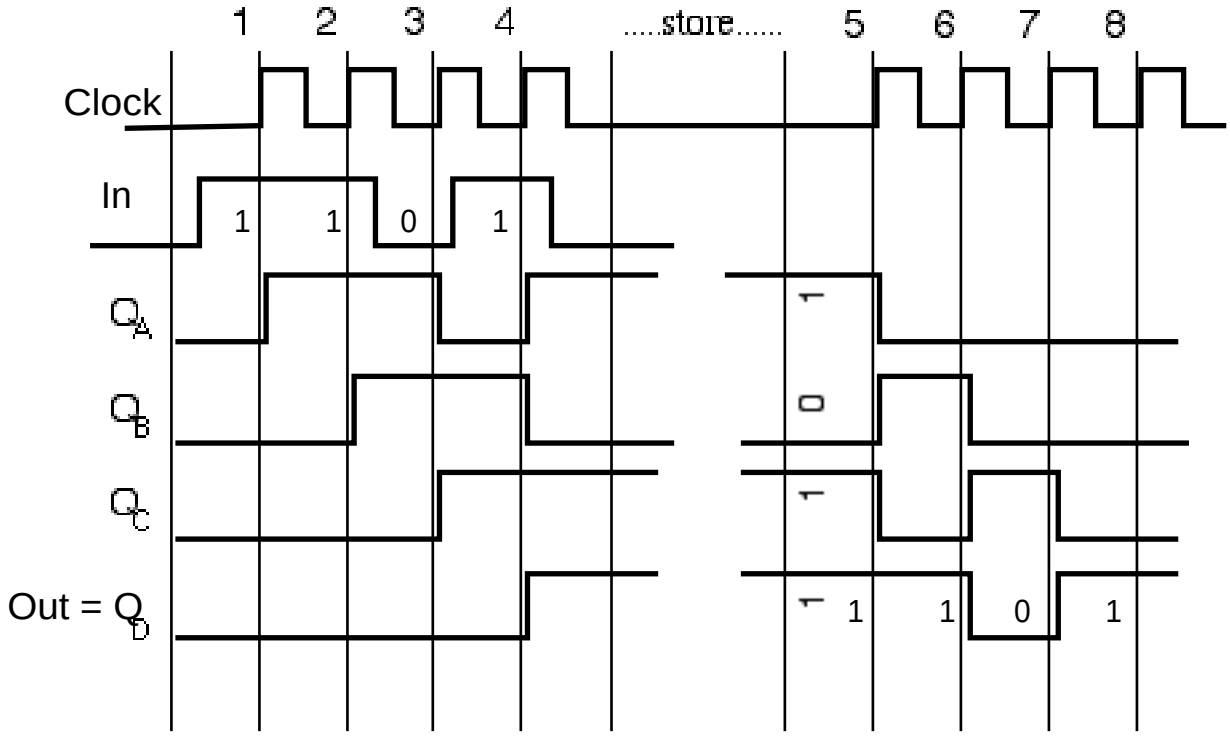
Exercise 6.1: Use the J-K flip-flop board or the counting and dividing board to construct a PIPO register. Note that you will need to use one of the flip-flops on the board as a clean pulse generator.

6.1.2 Serial-In Serial-Out (SISO)



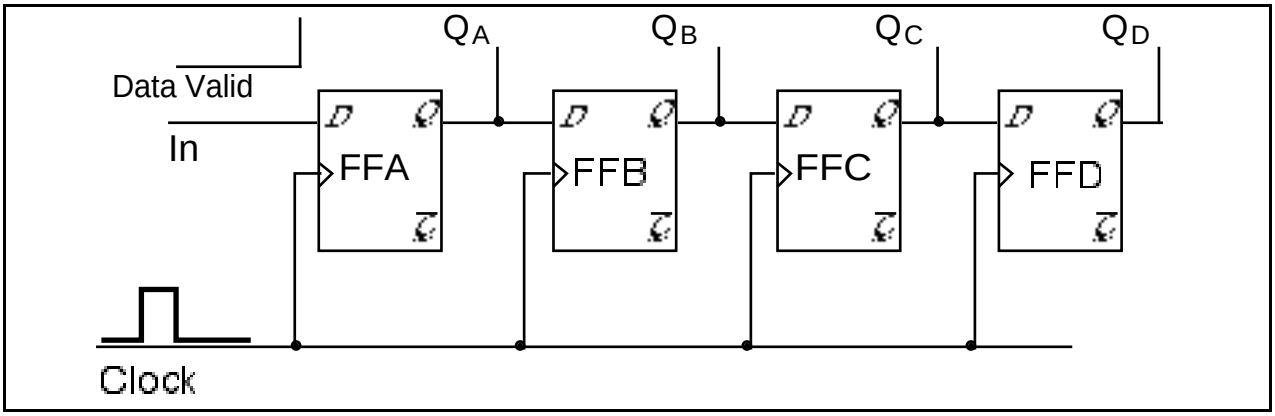
If data occurs serially in time – i.e. if the " bits" of data occur in a stream as is common in many communication applications – then there is a requirement to
(a) receive bits one at a time and then hold them in memory all together, and
(b) to send bits one at a time from a stored location.

The serial-in serial-out register achieves just this. The figure below (after Beards Figure 14.36) shows how the 4-bit number 1011 is treated as a serial data message (bits in time-reversed order!), being received in a register, held, and then read out.



Exercise 6.2: Use the J-K flip-flop board or the counting and dividing board to demonstrate the above use of a SISO register.

It would also be possible to read out the data in parallel if a separate line was provided to indicate when the data was valid, as below.

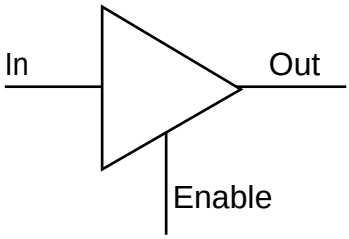


6.2 Tri-state Output

In the above SIPO register the states of the outputs are only "valid" at a certain moment (in other words, the four bits are in the correct order to correspond to the parallel version of the 4-bit serial input data). The "data valid" signal is therefore sent to the receiving circuit to tell it when to sample the parallel data. An alternative approach is to place "tri-state buffers" between the *Q* outputs and the lines sending the data to the receiving circuit. A tri-state buffer output has three electrical states instead of the usual two:

- "0" – usually a voltage close to zero
- "1" – usually a voltage close to +5
- "off" – the output terminal is effectively disconnected, usually described as being in a high impedance state.

The buffer has two inputs: one which determines the state of the output when it is "on": 0 or 1; the other, called the enable input, which switches the output "on" or "off". This is its circuit symbol:



Hence if the "data valid" signal is connected to the tri-state enable inputs, the register only has control over the output lines when the data is correct. At other times it is as if this register was disconnected from those lines. A more powerful use of the tri-state buffer is that it permits a given set of data lines (called a "data bus") to be controlled by many circuits. Provided only one of these circuits has its outputs enabled at any one time there will be no conflict due to different circuits trying to set the lines to different states simultaneously.

6.3 The digital/analogue interface

Although digital devices are nowadays ubiquitous there will always be a need for some circuits of the type known as "analogue". This is because the physical properties of the external world are not already encoded digitally: they have a continuously variable value. Examples would be the pressure of a sound wave arriving at a microphone or leaving a loudspeaker, or the intensity of light at a spot on a TV screen or at a point in the focal plane of a camera. Hence there is a need to process these signals electronically in a way that is compatible with their analogue nature and also a need to convert analogue signals to digital form and vice versa. Devices which perform these latter two functions are called "analogue to digital converters" and "digital to analogue converters" respectively, or ADCs and DACs for short.

An ADC should produce a digital binary coded output whose value is proportional to the value of the analogue signal present at its input, usually in the form of a voltage. The DAC obviously performs the reverse operation: it takes a digital binary coded input and generates a voltage at its output which is proportional to that input value.

6.3.1 The Digital to Analogue Converter

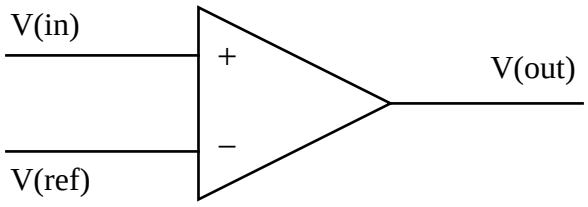
The DAC is little more than an accurately know voltage source – called a voltage reference – sent though a set of consecutive potential dividers whose very precisely manufactured resistors are switched in or out of circuit according to the binary values of the various bits of the digital input. We will not look in any further detail at the design of DACs but simply treat them as "black boxes".

6.3.2 Analogue to Digital Converters

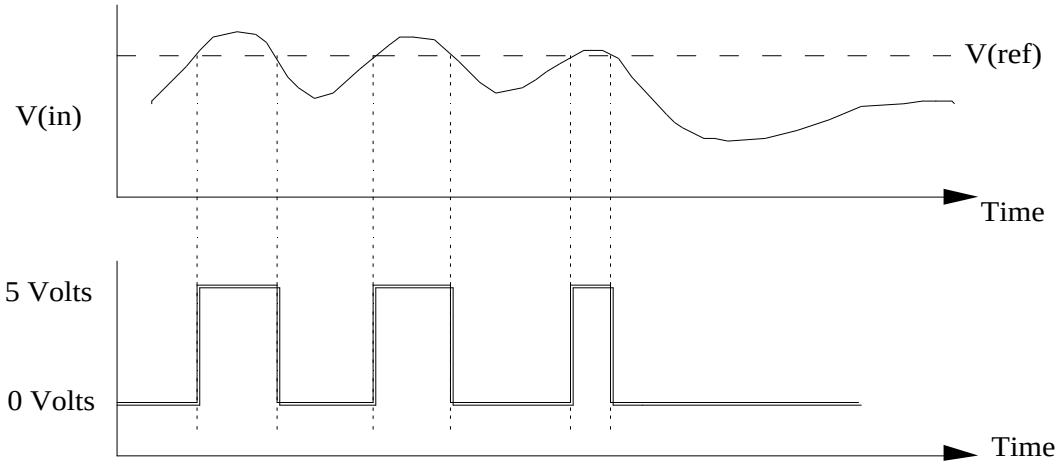
There are several types of ADC using different principles of operation. We will look at three types and highlight for which purposes each one is most appropriate. The common element of all these ADCs is a device known as an *analogue comparator.*

ANALOGUE COMPARATORS

The comparator is represented diagramatically by the following symbol…



What the circuit does is to compare an input voltage with a reference voltage. If $V_{in} < V_{ref}$ then the comparator has an output of logic 0 (often 0 Volts), but if $V_{in} > V_{ref}$ then the comparator has an output of logic 1 (often +5 Volts).



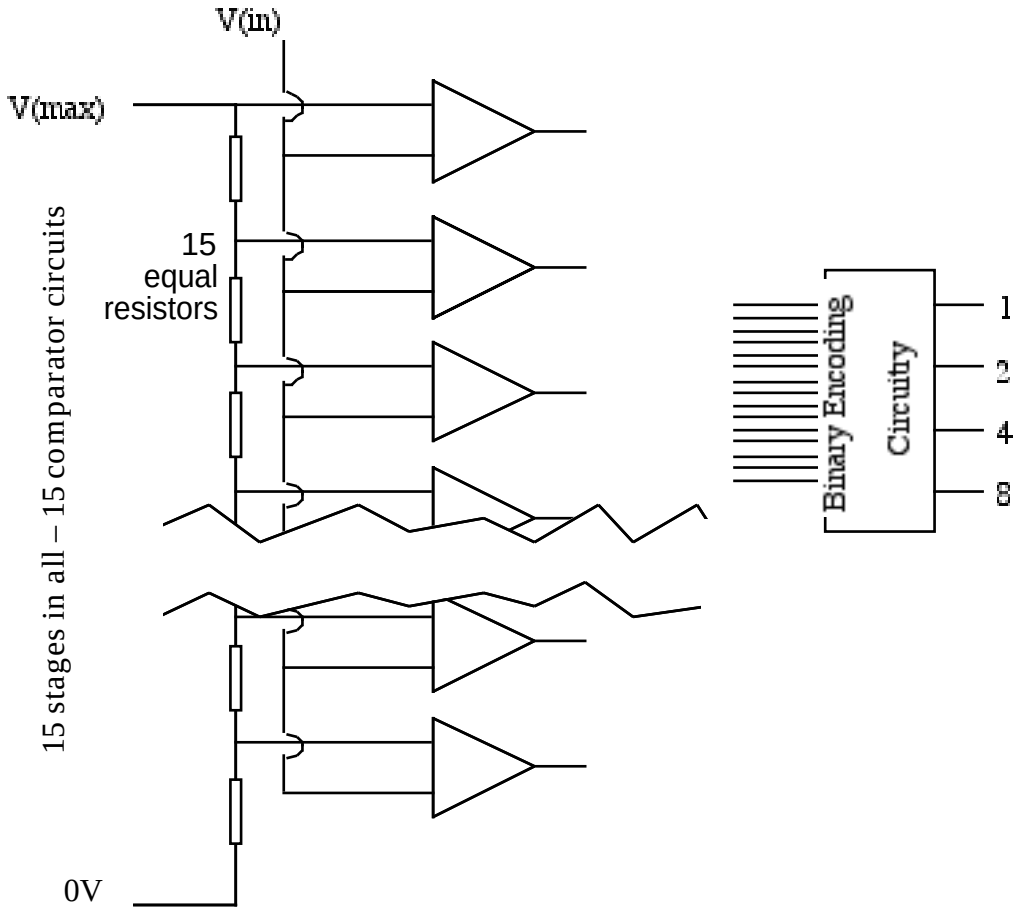
When $V_{in} = V_{ref}$ or when V_{in} and V_{ref} are very close together then the logical output of the comparator is not defined, i.e. the output is neither logic zero nor logic 1. A good comparator has a very narrow range (less than 1mV) of input voltages which produce indecisive results and more importantly can change from one state to the other very quickly. A fast comparator can switch in about 10 ns.

The comparator is the basic component for bridging between analogue and digital signals and is incorporated into all types of ADC but it plays a slightly different role in each device. All of the types of ADC we will consider are available as single integrated circuits or can be implemented as an integrated circuit plus a couple of discrete components. These are the devices around which digital voltmeters are built, for example. The three kinds of ADC are

- Parallel encoding or "flash" conversion,
- Successive approximation,
- Dual slope integration.

6.3.3 The Flash ADC

This device contains several comparator circuits and the input voltage is compared with several different voltages simultaneously. The reference voltages with which V_{in} is compared are derived from a fixed voltage representing the maximum voltage the converter will work with, V_{max}. In a “4-bit” device the input is compared with 15 voltages divided evenly over the range 0 to V_{max} generated from a simple chain of resistors. All the comparators with reference voltages greater than V_{in} will have outputs of logic 0. All the comparators with reference voltages less than V_{in} will have outputs of logic 1. This pattern of 15 0's and 1's is encoded into binary form to represent the input voltage. The time taken to do all this is just the time taken for a single voltage comparison plus the time taken to encode the results into binary format.



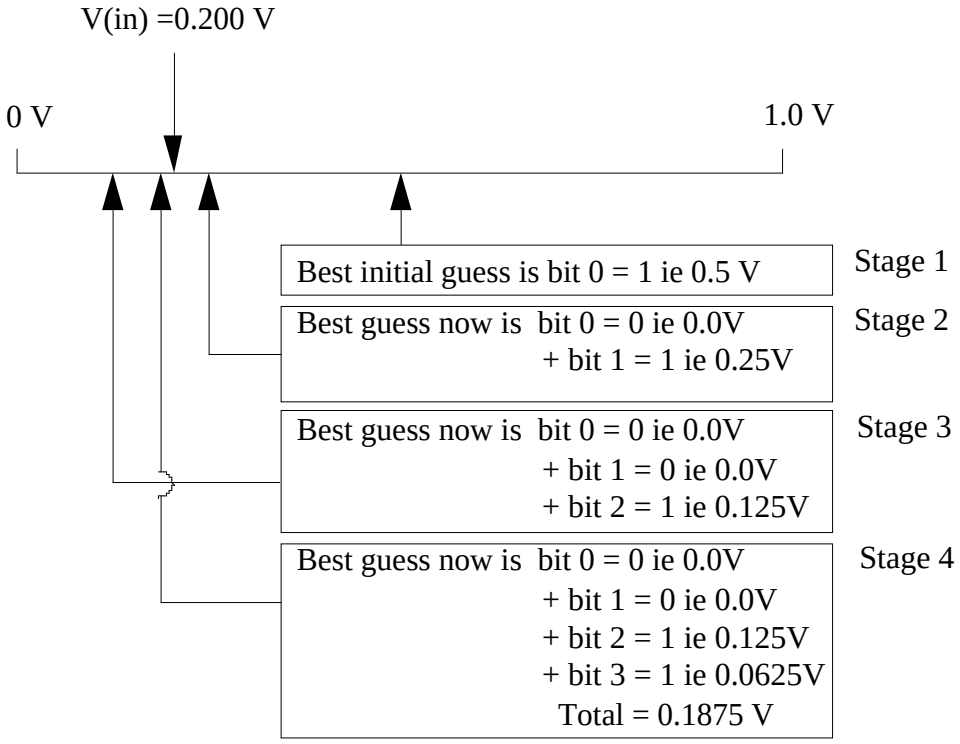
ADVANTAGES & DISADVANTAGES

- Performance. Flash converters are very fast and are used where speed is essential such as in measuring profiles of fast pulses.
- Cost. The comparator circuit must be carefully reproduced 2^n–1 times for an n-bit converter and in practice that limits the technique to 8 bits at most, i.e. 255 separate circuits giving a resolution of 1 in 255. Typical costs are from £30 to £130 for conversion times from 50 ns to 7 ns.
- Errors. Because of its mode of operation it is sometimes possible for flash converters to generate incorrect codes. This can be very important because a single bit can represent up to half of the maximum input.

6.3.4 The Successive Approximation ADC

In this device the input voltage is compared in turn with a succession of reference voltages derived from V_{max}. These voltages are generated by a more complex type of voltage divider called a *digital to analogue converter* (DAC) which turns a binary coded signal into a single voltage. For an *n*-bit converter the resolution is 1 in 2^n . The ADC makes *n* tries at the unknown voltage V_{in}, each time dividing in half the range of voltage within which V_{in} is known to lie.

Consider the example illustrated below of a 4-bit converter with a range of 0–1 V and an applied input voltage of 0.2 V. All bits are assumed to be 0 unless stated.



The resolution of the 4-bit ADC is $\Delta V = V_{max} / 2^4$.

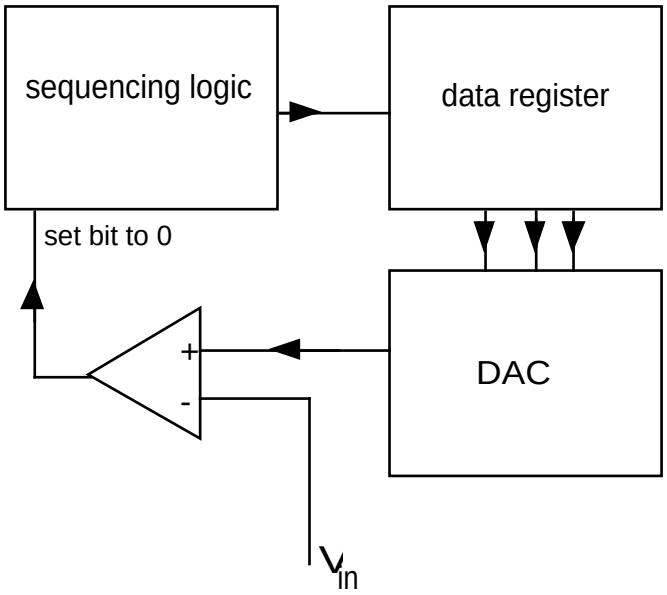
- Stage 1. The first try is always V_{in} is 0.5 V_{max}, i.e. $V_{max}/2$, represented by a *trial code* of 1000_b.
  If V_{in} is **greater than** $2^3 \times \Delta V$ then the first bit of the output code that represents $V_{max}/2^1$ (= $V_{max}/2$) is set to 1, i.e. the trial code remains 1000.
  If V_{in} is **less than** $2^3 \times \Delta V$ then the first bit of the output code that represents $V_{max}/2^1$ (= $V_{max}/2$) is set to 0, i.e. the trial code is reset to 0000.

- Stage 2. The second try is based in the results of the first comparison. We take the trial code generated from the first approximation and set the next bit of the code equal to 1 (i.e. either 1100 or 0100).
  If 1000 was the trial code generated by the first approximation (unlike the first example above) then in this second approximation…
  If V_{in} is **greater than** $(2^3+2^2) \times \Delta V$ then the second bit of the output code that represents $V_{max}/2^2$ (= $V_{max}/4$) is set to 1, i.e. the trial code for the next stage will be 1100.
  If V_{in} is **less than** $(2^3+2^2) \times \Delta V$ then the second bit of the output code that represents $V_{max}/2^2$ (= $V_{max}/4$) is set to 0, i.e. the trial code for the next stage will be 1000.

  If 0000 was the trial code generated by the first approximation (as in the first example above) then in this second approximation…
  If V_{in} is **greater than** $(0+2^2) \times \Delta V$ then the second bit of the output code that represents $V_{max}/2^2$ (= $V_{max}/4$) is set to 1, i.e. the trial code for the next stage will be 0100.
  If V_{in} is **less than** $(0+2^2) \times \Delta V$ then the second bit of the output code that represents $V_{max}/2^2$ (= $V_{max}/4$) is set to 0, i.e. the trial code for the next stage will be 0000.

- Stage 3,4,... This process is repeated until the least significant bit has been set or cleared.

We can represent the functionality of the ADC using a schematic diagram something like this:



ADVANTAGES & DISADVANTAGES

- Performance. Successive approximation ADCs are the most common type of ADC found in many cheap voltmeters, computer card type data acquisition systems, and digital audio equipment. They are slower and cheaper than flash ADCs because there is only one comparator circuit which has to operate many times for one conversion. They have resolutions of typically 8, 10, 12, 14 or rarely 16 bits. They work well at moderate speeds (1 µs to 50 µs being typical conversion times).

  8 bits at speeds of about 5 µs costs about £8
  10 bits at speeds of about 20 µs costs about £20
  12 bits at speeds of about 3 µs costs about £60
  12 bits at speeds of about 100 µs costs about £30

- Errors. In general modern successive approximation converters do not generate erroneous codes. However care must be taken about precisely when in the conversion cycle the output code becomes valid. There is usually a separate "Output Valid" connection on the device which tells one when to read the output.

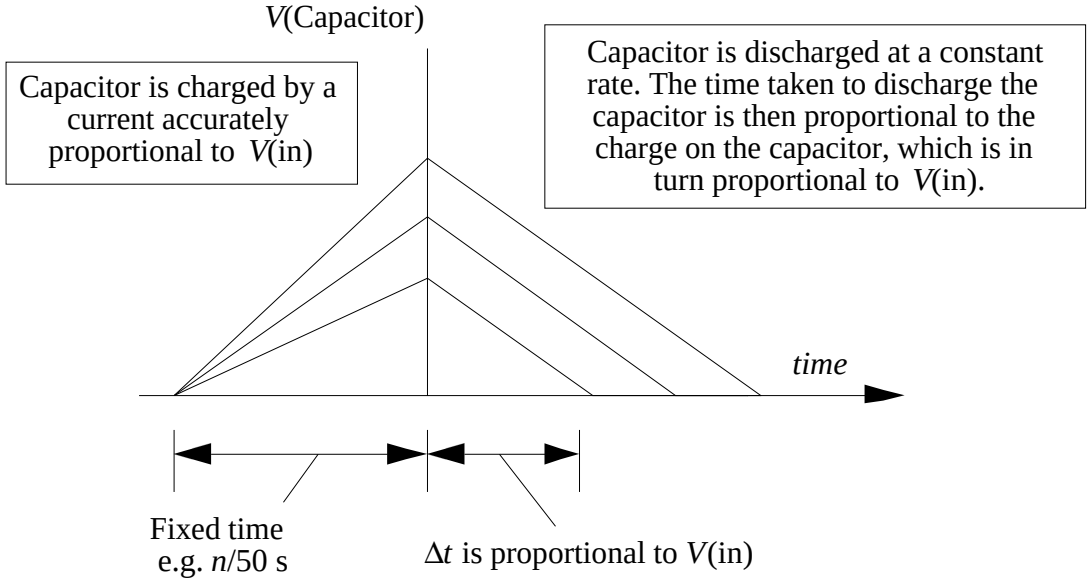
6.3.5 The Integrating ADC

An integrating ADC consists of three parts: an integrator, a comparator, and a clock. Many variations of this *charge balancing technique* exist and we shall look at just one of the techniques called *dual-slope integration*. There are three stages to the measurement.

- Firstly, a circuit generates a current accurately proportional to an input voltage. This is made to charge a capacitor for a fixed period of time (determined by a fixed number of clock cycles).

- Secondly, with the input disconnected, the capacitor is discharged by a constant current circuit until the voltage reaches zero, as determined by a comparator. The time taken for this discharge is measured by counting the number of regular clock pulses from an oscillator that occur during the discharge.

- Finally, the count of clock pulses is a number proportional to the magnitude of the input voltage. Digital circuitry can now convert this to the correct units.



This procedure has two characteristic properties. It is generally rather slow (typically 0.1 to 1 s/conversion) and rather precise, 15 or 16 bit resolution being typical and 20 bit resolution or better is possible. This device is found in most digital voltmeters with a reading of 2000 "units" or more.

ADVANTAGES & DISADVANTAGES

This technique has several outstanding features, and the main disadvantage is that the measurement is usually slower than other ADC techniques.

- Noise Rejection. All DC voltage measurements are accompanied by "noise" which makes the instantaneous voltage fluctuate about its mean value. The integration of the input signal over some period τ averages out noise fluctuations having a period much less than τ. In particular, if τ is made a multiple of (1/50) s, i.e. a multiple of 20ms, then voltages induced from the mains electricity supply are averaged to zero very precisely. This is very important.

- Accuracy has not been mentioned for the other types of ADC because they are not used for applications where very high accuracy (as opposed to speed or precision) is required. The dual slope integration technique has several features that give it the possibility of high accuracy. In particular, the final count is immune to long term changes in the capacitance or clock frequency because any drifts will cancel between the charging and discharging cycle. The device is intrinsically linear and precise. The accuracy depends on comparison of the counts from the unknown voltage with those from a calibrated voltage source. In a quality multimeter a long term accuracy of better than 1 in 10^4 is possible.

The cost of an integrated circuit is typically £20 for 16 bit resolution at 25ms per conversion. An accurate digital voltmeter with 18-bit resolution costs about £700–£1000. An accurate digital voltmeter with 23-bit resolution (1 in 10^6) costs from £1600-£5000.

- Errors. Because of the way the output code is generated by a counter there is a strictly monotonic variation of output code with input voltage. As with the successive approximation device one must make sure that one is reading the code at the appropriate point in the conversion cycle.

Exercise 6.3: Use *Crocodile Clips* to design a 2-bit flash ADC.